Exhibit A

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,	§	
	§	
Plaintiff,	§	
	§	
v.	§	CIVIL ACTION NO. 2:22-CV-00294-JRG
	§	
MICRON TECHNOLOGY, INC., *et al.*	§	[redacted]
	§	
Defendants.	§	

MEMORANDUM OPINION AND ORDER

Before the Court is the Rule 50(b) Motion for Judgment as a Matter of Law for Non-Infringement Regarding U.S. Patent Nos. 7,619,912 and 11,093,417 (the "Motion") filed by Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC. (collectively, "Micron" or "Defendants"). (Dkt. No. 159.) In the Motion, Micron moves for judgment as a matter of law of non-infringement for U.S. Patent Nos. 7,619,912 and 11,093,417 pursuant to Rule 50(b) of the Federal Rules of Civil Procedure. (*Id.* at 1.) For the reasons discussed herein, the Court finds that the Motion should be **DENIED**.

I. BACKGROUND

Plaintiff Netlist, Inc. ("Plaintiff" or "Netlist") alleged that Micron infringes claim 16 of U.S. Patent No. 7,619,912 (the "'912 Patent") and claims 1, 2, 8, 11–14 of U.S. Patent No. 11,093,417 (the "'417 Patent") (collectively, the "Asserted Patents"). (Dkt. No. 100; Trial Tr. at 1075:11-15.) After a trial in this case, the jury returned a unanimous verdict finding that Defendants infringed the Asserted Patents, that Defendants owed a total of $445,000,000 in damages for their infringement, and that Defendants willfully infringed the Asserted Patents. (Dkt. No. 135 at 4-6.) Micron now moves for judgment as a matter of law of non-infringement for the '912 and '417 Patents. (Dkt. No. 159 at 1.)

II. LEGAL STANDARD

"Judgment as a matter of law is proper when 'a reasonable jury would not have a legally sufficient evidentiary basis to find for the party on that issue.'" *Abraham v. Alpha Chi Omega*, 708 F.3d 614, 620 (5th Cir. 2013) (quoting Fed. R. Civ. P. 50(a)). The non-moving party must identify "substantial evidence" to support its positions. *TGIP, Inc. v. AT&T Corp.*, 527 F. Supp. 2d 561, 569 (E.D. Tex. 2007). "Substantial evidence is more than a mere scintilla. It means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Eli Lilly & Co. v. Aradigm Corp.*, 376 F.3d 1352, 1363 (Fed. Cir. 2004).

"The Fifth Circuit views all evidence in a light most favorable to the verdict and will reverse a jury's verdict only if the evidence points so overwhelmingly in favor of one party that reasonable jurors could not arrive at any contrary conclusion." *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 880 F.3d 1356, 1361 (Fed. Cir. 2018) (citing *Bagby Elevator Co. v. Schindler Elevator Corp.*, 609 F.3d 768, 773 (5th Cir. 2010)). A court must "resolve all conflicting evidence in favor of [the verdict] and refrain from weighing the evidence or making credibility determinations." *Gomez v. St. Jude Med. Daig. Div. Inc.*, 442 F.3d 919, 933 (5th Cir. 2006).

III. DISCUSSION

In the Motion, Micron moves pursuant to Rule 50(b) of the Federal Rules of Civil Procedure for judgment as a matter of law of non-infringement for the '912 and '417 Patents. (*Id.* at 1.) The Court begins by addressing the Motion as to the '912 Patent.

A. The '912 Patent

Micron contends that it is entitled to judgment as a matter of law of non-infringement as to (1) all accused products on the grounds that Netlist failed to prove that command signals are "transmitted to only one DDR memory device at a time," and as to (2) the accused dual-rank

RDIMM devices on the grounds that Netlist failed to prove that output signals control more devices and ranks than input signals. (Dkt. No. 159 at 1-2, 11.)

1. Micron's Motion for JMOL on All Accused Products on the Grounds that Netlist Failed to Prove that Command Signals are "Transmitted to Only One DDR Memory Device at a Time"

In the Motion, Micron asks the Court to grant judgment as a matter of law of non-infringement of the '912 Patent as to all accused products on the grounds that Netlist failed to prove "the command signal is transmitted to only one DDR memory device as a time," as recited by claim 16. (Dkt. No. 159 at 1, 6.) Micron contends, instead, that the undisputed evidence established that the command signal is not "transmitted to only one DDR memory device at a time" because the command signal is "transmitted to all memory devices" at a time. (*Id.* at 1, 7) (emphasis added). As support, Micron points out that Netlist's technical expert, Dr. Mangione-Smith, admitted that the command signals are transmitted "*towards* all DRAM memory devices" at the same time over a shared line (BUS) that connects all DRAMs in a rank. (*Id.* at 2 (citing Trial Tr. at 486:25-488:4) (emphasis added).)

Netlist responds that substantial evidence supports the jury's finding that the "transmitted to only one DDR memory device at a time" limitation is met. (Dkt. No. 173 at 1.) Netlist first argues that because the Court did not construe "transmitted to," the Court should defer to the "jury's view of the claim element unless that view is contrary to the only reasonable view of the claim element." (*Id.* (citing *VLSI Tech. LLC v. Intel Corp.*, 87 F.4th 1332, 1341 (Fed. Cir. 2023).) Netlist then argues that Micron's non-infringement argument hinges on the interpretation that "transmit to" means "transmit towards," which Netlist argues that the jury heard and rejected. (*Id.*) Specifically, Netlist points out that Dr. Mangione-Smith distinguished "transmitted to" from "transmitted towards" at trial, stating:

> Q. You don't believe that at the time the DRAM ignores the MRS command, that it's been sent to that DRAM?
>
> A. I don't believe that it's been transmitted to it. It's been transmitted maybe towards it in that direction but not to it.
>
> Q. Okay. So that's a little bit of a difference here.

(*Id.* at 4-5 (citing Trial Tr. at 486:20-25) (emphasis removed).) Consequently, Netlist contends that after Micron "invited the jury to decide whether the plain meaning of 'transmitted to' was 'transmitted towards,' the jury weighed the evidence and rejected" Micron's interpretation. (*Id.* at 5.)

Despite this evidence, Micron contends that Dr. Mangione-Smith interpreted the claim language "transmitted to" to require a transmission *and* receipt of the transmission. (Dkt. No. 159 at 2-3 (citing Trial Tr. at 489:23-25).) Micron argues that this interpretation is improper because (1) it adds limitations, such as "received," beyond the plain claim language "transmitted to," which the specification and claims use separately and distinctly from "transmit," and (2) no explanation was given as to how any intrinsic or extrinsic evidence supports Dr. Mangione-Smith's interpretation. (*Id.* at 8-9; *see also* Dkt. No. 178 at 2-3.) Nevertheless, Micron argues that even under Netlist's improper interpretation, the evidence at trial established that the command signal is transmitted to and received by every DDR memory device in a rank. (*Id.* at 3.)

Netlist responds that it is Micron who has attempted to rewrite the claim limitation by changing "transmitted to" to "transmitted towards." (Dkt. No. 173 at 4.) Notably, Netlist further responds that Micron never objected to Dr. Mangione-Smith's testimony as improper claim construction or as inconsistent with the plain meaning of the claims. (Dkt. No. 185 at 1 (citing Dkt. No. 178 at 2).) Regardless, Netlist argues that Dr. Mangione-Smith did not attempt to write additional limitations into the claims; rather, he applied the plain and ordinary meaning of "transmitted to" in his infringement analysis. (Dkt. No. 173 at 6.) As support, Netlist emphasizes several pieces of evidence showing infringement under the plain and ordinary meaning. (*Id.* at 6.)

For example, Netlist points out that Dr. Mangione-Smith explained to the jury that it is the per-DRAM addressability ("PDA") mode functionality of the accused products that enables MRS commands to be transmitted to a single DRAM on a rank. (*Id.* at 6 (citing Trial Tr. at 357:20-364:24, 505:22-508:23).) Netlist also points out that it was Micron's corporate representative, Mr. Ross, who testified that PDA mode is "used for accessing -- or addressing only a single DRAM device at a time." (*Id.* at 6 (citing Trial Tr. at 537:20-23).) Moreover, Netlist notes Dr. Mangione Smith testified that even though other DRAMs shared some common signal lines, the MRS command would be transmitted only to the selected DRAM. (*Id.* at 6 (citing Trial Tr. at 508:9-23).) Netlist also points out that only one DRAM will receive the command and do what the command says as a result of this transmission of a command signal to a single DRAM. (*Id.* at 6 (citing Trial Tr. at 360:16-361:21).)

Micron argues, however, that even if the plain meaning of "transmitted to" included "received by," the evidence established that the MRS command is transmitted to and received by "every" DDR memory device. (Dkt. No. 159 at 3; Dkt. No. 178 at 3.) As support, Micron cites Dr. Mangione-Smith's testimony that the MRS commands are transmitted before the DQ0 signals (which put the memory device receivers into standby mode) are transmitted. (*Id.* at 3 (citing Trial Tr. at 440:22-24; 471:21-24; 477:5-7; 508:9-19).) Micron further contends that Dr. Stone explained how the process for exiting PDA mode demonstrates that the memory devices receive commands even while in PDA mode. (*Id.*) Consequently, Micron argues it is unreasonable to assume the accused command signals are not transmitted to and received by each DRAM when the evidence shows that the DQ0 signals, which turn off some DRAMS and activate one of the DRAMs, do not arrive until after the MRS commands have already been sent. (*Id.* at 9-10 (citing Trial Tr. at 675:21-676:16); *see also* Trial Tr. at 508:9-23; Dkt. No. 178 at 3).)

In response, Netlist cites Dr. Mangione-Smith's testimony that the command signal has not been "transmitted to" any of the DRAMs "until the point in time when the DQ0 signal turns off some DRAMS and activates one." (Dkt. No. 173 at 4 (citing 507:17-508:23; *see also* 362:8-10 ("[JX-9] tells me that the MRS commands are qualified with DQ0. That means if DQ0 is not set low, the DRAM chip is not going to receive and execute that MRS command.").) Netlist argues that this is consistent with the specification's description stating that "[t]his is an embodiment in which only one device does what the command says." (*Id.* at 6-7 (citing Trial Tr. at 725:16-726:8).) Further, Netlist points out that Micron's argument about exiting PDA mode improperly focuses on Step 3 ("Take DRAM out of PDA mode"), instead of Step 2 ("Program the unique DRAM locations by using posted MRS commands, address inputs and DQ[0]."). (Dkt. No. 185 at 3.) Ultimately, Netlist contends that substantial evidence supports the jury's finding that PDA mode infringes the "transmitted to" limitation of claim 16. (*Id.*)

After reviewing the evidence, the Court finds that substantial evidence supports the jury's finding that the "transmitted to only one DDR memory device at a time" limitation is met. As a preliminary matter, the Court did not construe that term and therefore defers to the jury's view of the plain and ordinary meaning of the claim element unless that view is contrary to the only reasonable view of the claim element. *See VLSI Tech. LLC*, 87 F.4th 1332 at 1341; *see also Solas OLED Ltd. v. Samsung Display Co.*, No. 2:19-CV-00152-JRG, 2021 WL 4950308, at *11 (E.D. Tex. Oct. 25, 2021) ("The Court initially notes that 'connected' was not construed by the Court and the jury was instructed to apply the plain and ordinary meaning. The Court also finds that Plaintiff presented sufficient evidence on this issue. Mr. Credelle testified that the claim limitation was met."). In this case, Micron's non-infringement argument hinges on the interpretation that "transmit to" requires only being "transmitted towards." (Dkt. No. 159 at 1.) Since the Court does

not find that "transmitting towards" is the "only reasonable view" of the claim element "transmitting to," the Court defers to the jury's view of the claim. *See VLSI Tech. LLC*, 87 F.4th 1332 at 1341; *Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1048 (Fed. Cir. 2016) ("The case went to the jury without a construction of the key 'in files' language, and Avid has not met its burden of showing that it has the only reasonable view of the claim element as long as it is un-construed.").) Here, after hearing Micron's argument, the jury rejected it.

Moreover, in addition to the testimony already discussed above, the jury heard testimony from several witnesses, including Dr. Mangione-Smith, Mr. Frank Ross, and Dr. Harold Stone, that would allow them to conclude that claim 16 was infringed. Dr. Mangione-Smith, for example, cited a Micron document discussing PDA mode (JX-9) and testified that "a number of reasons" demonstrate that "Micron's devices transmit command signals to only one DDR memory device at a time." (Trial Tr. at 506:1-8.) The jury heard Dr. Mangione-Smith testify that JX-9 states that PDA mode allows Micron's devices to "program devices individually." (*Id*. at 506:8-9.) The jury heard evidence that individual programmability would not have been possible if the MRS command were transmitted to all the devices on a rank as opposed to only one device at a time. (*Id.* at 506:13-16.) The jury also heard evidence from Dr. Mangione-Smith that the "DQ0 [signal] is used to control which individual DRAM the MRS message is transmitted to" such that the command signals are not transmitted to any of the DRAMs until the DQ0 activates one DRAM. (*Id.* at 507:14-21.) The jury could have reasonably found that a command signal is not "transmitted to" a DDR memory device unless "the command signals in PDA mode are addressed to a single DRAM device" and the device receives them.[1] (*Id.* at 507:6-9.)

[1] The Court notes that counsel for Micron used an analogy during its cross-examination of Dr. Mangione-Smith that was focused on the claim limitation "transmitted to" as compared with the same limitation when characterized as "transmitted towards." (*See, e.g.,* Trial Tr. at 488:10-490:3.) In that analogy, counsel for Micron asked whether he would have "transmitted [envelopes] to" all twenty people in Dr. Mangione-Smith's neighborhood if counsel had

The jury also heard testimony from Micron's own witnesses, Frank Ross, Scott Cyr, and Dr. Stone, that would enable them to conclude this limitation was satisfied. For example, Mr. Ross testified that when a DRAM is not selected, its receiver for the command and address signals are disabled, and that DRAM does not receive any command signal. (Trial Tr. at 529:20-25; *see also* Trial Tr. at 530:13-18 ("Q. And so in the per-device addressability mode, the selected DRAM will receive the command address signal while the ones that's not -- that are not selected will have their receivers in the standby mode and ignore the command address signals. Is that correct? A. That's right.").) Likewise, Dr. Stone admitted that "it's possible in PDA mode to tell one device in a rank and one device only to execute that MRS command." (Trial Tr. at 731:10-12.) Finally, Mr. Cyr, a Micron engineer designated as a 30(b)(6) witness on technical issues, testified that in PDA mode "if the rank activated for the MRS command, if only device has its DQ0 low, that will be the only device to accept the MRS commands." (Dkt. No. 560:10-15.) Based on the testimony from Mr. Ross, Dr. Stone, and Mr. Cyr, the jury could reasonably reject the argument that the command signals are transmitted to all devices and conclude that command signal is selectively transmitted only to specific devices.

Ultimately, the Court finds that substantial evidence supports the jury's finding that the command signals are transmitted to only one DDR memory device at a time. Accordingly, the Court finds that judgment as a matter of law for non-infringement of the '912 Patent is not appropriate under Micron's "transmitted towards" argument.

addressed the envelopes and put them in the mail. (*See id.* at 489:18-21.) Dr. Mangione-Smith confirmed that counsel may have transmitted them "towards" everyone in the neighborhood, but he would not have transmitted them "to" everyone in the neighborhood unless the addressees actually receive them. (*See id.* at 489:18-25.) After hearing Micron's analogy, the jury could have concluded, under the plain and ordinary meaning of "transmitted to," that the command signals were transmitted to only one DDR memory device at a time as recited by claim 16.

2. Micron's Motion for JMOL on the Dual-Rank RDIMM Products on the Grounds that Netlist Failed to Prove Claim 16's Requirement that Output Signals Control More Devices and Ranks Than Input Signals

With respect to only the accused dual-rank RDIMM products, Micron contends it is entitled to judgment as a matter of law of non-infringement of the '912 Patent for a second, independent reason. (Dkt. No. 159 at 11.) Specifically, Micron contends that neither of Netlist's two infringement theories can satisfy claim 16's requirement that input signals controlling a second number of ranks be smaller than the first number of ranks controlled by the output signals. (Dkt. No. 159 at 1, 11; JX-02.45.)

Claim 16 of the '912 Patent recites, *inter alia*:

> a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks

(JX-02.45, '912 Patent Claim 16).

Micron claims that Netlist's primary infringement theory for the accused quad-rank devices, which relied on Encoded Quad Chip Select ("QuadCS") mode, fails as to the dual-rank devices because Netlist presented no evidence that the dual-rank devices use the Encoded QuadCS mode and the undisputed evidence demonstrated that the dual-rank devices lack the required connectivity/wires to operate in Encoded QuadCS mode. (*Id.* at 1-2.) Micron also claims that Netlist's alternative infringement theory based on single-rank MRS command mode fails because it relates to LRDIMM products, not RDIMM products, and because it mixes and matches features

from two distinct modes—i.e., single-rank MRS command mode and PDA mode—that do not work together. (*Id.* at 2.)

Netlist responds that a reasonable jury could find that claim 16's requirement that the RCD provides output signals that control a greater number of memory devices and ranks than input signals is met by the accused dual-rank RDIMMs based on either of its two independent theories presented by Dr. Mangione Smith. (Dkt. No. 173 at 2.)

Regarding its single-rank MRS command theory, Netlist contends that Micron's Motion simply presents waived attorney arguments that are procedurally improper and substantively insufficient to overturn the jury's verdict as attorney arguments are not evidence. (*Id.*) Further, Netlist contends that Dr. Mangione-Smith explained why the limitation was met under the single-rank MRS command theory, and Dr. Stone admitted he did not dispute that theory at trial. (*Id.*) Netlist claims that a reasonable jury, therefore, could conclude that Micron did not dispute the infringement under the single-rank MRS command theory and find infringement accordingly. (*Id.*)

Regarding its Encoded QuadCS mode theory, Netlist contends that Micron not only improperly reurges its failed summary judgment argument, but that a reasonable jury could accept Dr. Mangione-Smith's explanation that the RCD on a dual-rank RDIMM is configured to support the Encoded QuadCS mode because the RCD would not know beforehand which configuration the memory controller will place the memory module in and has to support whatever configuration is set by the memory controller. (*Id.*)

The Court now addresses whether there is substantial evidence to support the jury's infringement verdict under either theory:

a. The Single-Rank MRS Command Theory

Netlist contends not only that there is substantial evidence that dual-rank RDIMMs infringe based on the single MRS command theory, but that this theory is sufficient for the Court to uphold

the jury's infringement verdict as to the '912 Patent. (Dkt. No. 173 at 18-19 (citing *Innovation Scis., LLC v. Amazon.com, Inc.*, No. 2021-2111, 2022 WL 2824675, at *2 (Fed. Cir. July 20, 2022), cert. denied, 143 S. Ct. 779 (2023) ("When a jury returns a general verdict for which there are multiple independent factual bases, however, a lack of substantial evidence for some of those bases does not warrant JMOL.") (citing *Walther v. Lone Star Gas Co.*, 952 F.2d 119, 126 (5th Cir. 1992) ("[W]e will not reverse a verdict simply because the jury might have decided on a ground that was supported by insufficient evidence."); *Northpoint Tech., Ltd. v. MDS Am., Inc.*, 413 F.3d 1301, 1311 (Fed. Cir. 2005) ("[E]ven if some of the proposed factual grounds for liability are not legally sufficient to support a verdict, that is not fatal, because the critical question is whether the evidence, taken as a whole, was sufficient to support the jury's verdict." (collecting cases)).) Netlist contends, in other words, that the Court "must uphold the verdict if substantial evidence supports *any* of the proffered factual bases." *Innovation Scis., LLC*, 2022 WL 2824675, at *2.

Under this first theory, Netlist contends that Dr. Mangione-Smith presented unrebutted evidence that the single-rank MRS commands satisfy the limitation for all accused products. (Dkt. No. 173 at 13.) Specifically, Netlist contends that Dr. Mangione-Smith testified that the single-rank MRS commands for multi-rank settings meet the disputed limitation in all accused products and Micron chose not to cross him on this issue. (*Id.* (citing Trial Tr. at 352:9-17; *see also* 431-504 (cross); 525-527 (re-cross).) Netlist also contends that Micron chose not to have its own expert, Dr. Stone, address this issue. (*Id.* (citing Trial Tr. at 747:13-15 ("Q. You said absolutely nothing about Doctor Mangione-Smith's analysis of a single-rank MRS command capability. Correct? A. That is correct.").) Netlist contends that given Micron's silence on this theory during trial, the jury could have reasonably found infringement under the uncontested single-rank MRS command theory. (*Id.*)

In its Motion, Micron argues that this theory fails because "all the evidence at trial related only to 'LRDIMM applications,' not dual-rank RDIMM applications." (Dkt. No. 159 at 17; *see also id.* at 2 ("Netlist's alternative infringement theory, using a single-rank MRS command mode, relates to LRDIMM products, not RDIMM products.").) Specifically, Micron argues that Dr. Mangione-Smith attempted to prove that Micron's accused products use single-rank MRS mode commands by identifying Table 12 and its footnote from DX-29 at 43. (Dkt. No. 159 at 18.)

While nothing in Table 12 or the footnote limits this to LRDIMM applications, Micron argues that it is applicable only to LRDIMM applications because it is part of a section titled "DQ Bus Termination in LRDIMM application." (*Id.* (citing DX-29 at 41).) Micron further argues that though Dr. Mangione-Smith cites exhibits PX-5a-c as support for his theory, each of these exhibits also identify that they are applicable only in LRDIMM applications. (*Id.* (citing PX-5a.48-50; PX-5b.25-27; PX-5c.31-33).) Furthermore, Micron argues that "single-rank MRS commands are used to configure the BODT setting in ***data buffers*** found only in LRDIMMs, thus confirming such commands are only applicable to LRDIMM applications." (*Id.* (citing DX-29.41-42) (emphasis original) (footnote omitted); Dkt. No. 178 at 5 ("RDIMMs do not have data buffers.") Micron claims, therefore, that Dr. Stone did not address this alternative theory because Netlist did not carry its burden in the first instance. (Dkt. No. 159 at 18; Dkt. No. 178 at 5.)

Netlist responds that nothing in the document actually states that the table presented to the jury is applicable only to LRDIMs. (Dkt. No. 173 at 14; Dkt. No. 185 at 5-6.) Netlist further responds that while Micron argues that a "BODT" (i.e., Buffer On-Die Termination) setting relates to data buffers and thus is only configured in LRDIMM products, Table 12 describes how RCD

[redacted] (*Id.* at 15) (emphasis original).)

Micron next argues that the single-rank MRS command mode theory fails because the record establishes that dual-rank RDIMMs are not "reasonably capable" of implementing single-rank MRS commands using the *TGIP* factors. (Dkt. No. 159 at 19.) Specifically, Micron argues that the dual-rank RDIMMs are not reasonably capable of using single-rank MRS commands because (1) the evidence shows that Micron and other industry participants did not intend or anticipate that customers would modify the accused device to operate in an infringing manner, (2) no evidence shows that Micron's RDIMMs were ever designed to be altered or assembled to use single-rank MRS commands, (3) the technical documents only demonstrate that LRDIMM, not RDIMM, products implement single-rank MRS command mode and confirm that RDIMMs would not actually operate or in any way use such commands, and (4) no evidence shows that single-rank MRS commands would serve any purpose in RDIMM applications given those commands configure settings in data buffers found only in LRDIMMs, not RDIMMs. (*Id.*) Consequently, Micron argues that none of the evidence Netlist presented supports that the dual-rank RDIMMs are reasonably capable of using single-rank MRS commands, which Micron claims are used only in LRDIMM applications to configure buffers that RDIMMs do not have. (*Id.* at 20.)

Netlist responds that Micron "failed to present any counter-evidence at trial" and now "resorts to post hoc attorney arguments on theories disclosed for the first time in its motion." (Dkt. No. 173 at 13-14.) Netlist notes, for example, that Dr. Stone's rebuttal report does not contend that the disclosure relied on by Dr. Mangione-Smith applies only to LRDIMMs, and not to RDIMMs. (*Id.* at 14.) Netlist further notes that Dr. Stone did not opine that single-rank MRS commands are used to configure the BODT setting in data buffers found only in LRDIMMs. (*Id.*) In sum, Netlist contends that the jury neither heard nor saw evidence supporting Micron's new interpretation or rebutting Dr. Mangione-Smith's testimony. (*Id.*) Netlist contends, therefore, that

Micron is "asking the Court to make a *de novo* assessment of a technical document based on Micron's post-trial attorney argument," which is no substitute for its expert's testimony. (*Id.* (citing e.g., *Invitrogen Corp. v. Clontech Lab'ys, Inc.*, 429 F.3d 1052, 1068 (Fed. Cir. 2005) ("Unsubstantiated attorney argument regarding the meaning of technical evidence is no substitute for competent, substantiated expert testimony."); *see also Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1259–60 (Fed. Cir. 2010) ("Becton never argued at trial that Boyce's force displacement test showed that the hinges contributed in any way to the movement of the guard. No witness, either on direct or cross-examination, testified that Boyce's tests reflected any such movement. Unsupported attorney argument, presented for the first time on appeal, is an inadequate substitute for record evidence.").)

Netlist contends, instead, that the jury heard substantial evidence that the single-rank MRS commands meet the limitation at issue in claim 16. (*See* Dkt. No. 173 at 12-18.) Netlist notes that Dr. Mangione-Smith began by explaining what MRS commands are and their general use in the accused products. (*Id.* at 15 (citing Trial Tr. at 348:12-349:23).) Dr. Mangione-Smith then presented an example of using MRS commands to set the DRAM chips' burst lengths to demonstrate infringement. (*Id.* (citing Trial Tr. at 349:24-350:12).) He testified that the input signals of the disputed limitation are met, for example, by the host sending an MRS command to set the burst length of the devices in rank 0. (*Id.* (citing Trial Tr. at 350:13-19).) He further testified that the JEDEC RCD specification and third-party RCD data sheets states that the RCD "assumes that all ranks are configured identically for certain values," which include "Write/Read Pre-amble, Burst length, and Write CRC," and "may monitor DRAM MRS commands for only rank 0." (*Id.* at 16 (citing Trial Tr. at 350:20-351:12; DX-29).) Dr. Mangione-Smith further explained that the "burst length setting for rank 0 is used to control the burst length setting for all of the ranks because

they have to all be the same. And there's one thing I know for sure is that each DIMM at least has a rank of 0." (*Id.* at 17 (citing Trial Tr. at 352:9-20).) Accordingly, Netlist contends that this demonstrates that Dr. Mangione-Smith's testimony "applies to all DIMMs at issue, and not just the LRDIMMs." (*Id.*) Netlist claims, therefore, that there is substantial evidence that Micron's dual-rank RDIMMs are reasonably capable of implementing single-rank MRS commands, particularly given that "no contrary evidence was presented to the jury." (*Id.*)

In Micron's final argument as to why the single-rank MRS command mode theory fails, Micron contends that Netlist improperly mixes technical features from two distinct modes. (Dkt. Nos. 159 at 20; 178 at 6-7.). Specifically, Micron argues that Dr. Mangione-Smith improperly relied on signals transmitted in the distinct PDA mode for infringement. (*Id*.) Micron contends it was improper to rely on commands from two distinct modes because the limitations require that the claimed "circuit" respond to the claimed command signal and input signal from the same command, and Netlist did not demonstrate whether the two modes can operate concurrently. (*Id.*)

Netlist contends, once again, that Micron made no such assertion at trial and now presents only waived attorney arguments that are procedurally improper. (Dkt. Nos. 173 at 2, 17; 185 at 6.) Netlist also contends that Micron is mistaken because the claim "does not preclude the command signals from being sent to different ranks of DRAM devices at different times." (*Id.* at 17.) Though single-rank MRS commands control all ranks, Netlist contends this does not mean the commands are transmitted to all devices at once. (*Id.*) As an example, Netlist contends that after a particular rank is placed into PDA mode, a MR4 command can selectively set a DRAM. (*Id.* at 18.) Accordingly, Netlist contends that there is sufficient evidence to support the jury's verdict. (*Id.*)

Ultimately, the Court finds that there is substantial evidence that dual-rank RDIMMs infringe based on the single-rank MRS command theory. In addition to the evidence cited above,

the jury heard from Dr. Mangione-Smith that there are "other ways that Micron infringes the claim that don't require it to use encoded quad chip select mode" that are "completely independent from the encoded quad chip select mode." (Trial Tr. at 348:5-10.) The jury heard that Dr. Mangione-Smith referred to this theory as "using a single MRS command to settings for multiple ranks." (Trial Tr. at 348:11.) After jury heard that MRS command stands for "mode register set" and is a command that "gets sent from the memory controller to the RCD and then propagates onward," Dr. Mangione-Smith testified that Micron's documents show that Micron's modules use these commands. (Trial Tr. at 348:12-24.) He explained that the MRS commands can be used, for example, to set "burst length," which is when individual DRAMS send four or eight chunks of data. (Trial Tr. at 350:1-9.) The jury then heard that a "JEDEC specification," marked as exhibit DX-29, states that the "RCD assumes that all ranks are configured identically with regards to certain values, one of which is burst length" and that Micron "implement[s] this functionality into its products." (Trial Tr. at 351:1-15.) The jury further heard Dr. Mangione-Smith testify that he knows Micron implements this functionality into its "RDIMM products and the LRDIMM products," because exhibits JX 4 and JX 5 state that Micron's devices comply with the JEDEC specification. (Trial Tr. at 351:16-352:17.) Furthermore, evidence presented to the jury showed that there were no material differences between RDIMMs and LRDIMMs for infringement of claim 16 of the '912 Patent. (*See, e.g.,* Trial Tr. at 331:20-332:14 ("Q. Does Micron sell a variety of different RDIMM products and LRDIMM products? A. Yes. Q. Does your infringement analysis apply equally to all those products? A. Yes. There are no differences among them that affect my opinion."); 333:18-19).) The jury was also presented with evidence from Table 12 describing how RCD [redacted]

[redacted]) Having considered the totality of the evidence presented to the jury in this case, the Court rejects Micron's argument that all the evidence at trial related only to LRDIMM applications, not dual-rank RDIMM applications.

The Court also agrees with Netlist that Micron failed to present any counter-evidence at trial and now resorts to post hoc attorney arguments on theories disclosed for the first time in its Motion. Notably, Micron cites to no evidence in the record presented to the jury establishing that the single-rank MRS command applies only to LRDIMMs, and not to RDIMMs.[2] Consequently, the jury neither heard evidence or testimony rebutting Dr. Mangione-Smith's testimony on this theory nor did Micron present this theory to the jury. (*Id.*) The Court will not make a *de novo* assessment now based on Micron's post-trial attorney argument, which is no substitute for the evidence presented to the jury for their consideration at trial. *See Becton, Dickinson & Co.*, 616 F.3d at 1259–60 ("Becton never argued at trial that Boyce's force displacement test showed that the hinges contributed in any way to the movement of the guard. No witness, either on direct or cross-examination, testified that Boyce's tests reflected any such movement. Unsupported attorney argument, presented for the first time on appeal, is an inadequate substitute for record evidence.").)

Accordingly, the Court finds that Netlist's single-rank MRS command theory is sufficient for the Court to uphold the jury's finding of infringement of the accused dual-rank RDIMMs. The Court will, nevertheless, address whether Netlist's encoded QuadCS mode theory is also sufficient to uphold the verdict.

[2] Micron claims that Dr. Stone did not discuss whether dual-rank RDIMM products are configured to implement single-rank MRS command mode because Netlist had only presented evidence regarding "LRDIMM (*i.e.,* not RDIMM) products." (Dkt. No. 159 at 6.) While Micron could easily have presented this contention to the jury at least once, Micron points to no such evidence in the record.

b. The Encoded QuadCS Mode Theory

Netlist contends that though substantial evidence supports the jury's finding of infringement of dual-rank RDIMMs based on the single MRS command theory and is sufficient for the Court to uphold the verdict, there is also substantial evidence in the record supporting a finding the accused products are capable of utilizing Encoded QuadCS mode. (Dkt. No. 173 at 18.)

As support, Netlist points to Dr. Mangione-Smith's testimony at trial that Micron's RDIMM and LRDIMM datasheets explain that all RDIMMs and LRDIMMs are capable of using Encoded QuadCS mode:

> Q. And so is it your understanding that Micron and its expert are taking the view that at least some of their memory modules simply cannot use encoded quad chip select mode?
>
> A. Yes, I recall hearing that.
>
> Q. Do you agree with that?
>
> A. No.

[redacted]

(Dkt. No. 173 at 19 (emphasis original) (citing Trial Tr. at 346:14-347:1). Additionally, Netlist notes that, on cross-examination, Dr. Stone confirmed that Micron's datasheet for its RDIMM products discusses [redacted].[3] (*Id.* at 21 (citing Trial Tr. at 744:14-20 ("Q. Sure. This is Micron's data sheet for its RDIMM products. Correct? A. That's correct. [redacted] Micron contends that Netlist's expert "blatantly mischaracterizing a clear statement in a document like this is not substantial evidence." (*Id.*)

Netlist also points to Dr. Mangione-Smith testimony at trial where he explained that the dual-rank RDIMMs are capable of using Encoded QuadCS mode because the "module" is controlled by the "memory controller," which is sometimes referred to as the "host," and "if the host tells it to go into encoded quad chip select, it will do it." (Dkt. No. 173 at 20 (citing Trial Tr. at 347:2-14).) He further explained that he was not "aware of any RDIMM or LRDIMM that Micron sells that doesn't have this capability to use encoded quad chip select mode" because "all" the RDIMMs and LRDIMMs "use the same RCD, and so their RCDs can be programmed in exactly that [encoded quad select] mode." (*Id.* (citing Trial Tr. at 347:18-23).) As further support, Netlist notes that Dr. Mangione-Smith discussed testimony from Mr. Cyr to prove his point that "[i]f the host wants the device to go into encoded quad chip select mode, it will do that." (*Id.* (citing Trial Tr. at 347:24-348:4); *see also* Trial Tr. at 558:9-14 ("Q. Are there any RDIMM or LRDIMMs

[3] Netlist notes that though the LRDIMMs and RDIMMs use the same RCDs, Micron's Motion does not dispute that its dual-rank LRDIMMs are configured to use the Encoded QuadCS mode. (Dkt. No. 173 at 21.) Micron responds that it does dispute this, but chose to limit the issues raised in post-trial briefing so as to focus the Court's review solely on dual-rank RDIMMs. (Dkt. No. 178 at 9.)

that Micron sells that don't have the capability of per-DRAM addressability or quad mode CS if the host instructs them to use it? A. [Mr. Cyr:] Again, we wire the device per the JEDEC specification, and that -- that follows the -- the raw card, and it's – it's up to the host to decide.").[4]

Despite this evidence, Micron argues that the "evidence shows that it is impossible for Micron's dual-rank RDIMMs to use the allegedly infringing encoded quad chip select mode because these modules do not have the necessary wiring." (Dkt. No. 159 at 12.) Specifically, Micron argues that its "***dual***-rank RDIMMs" do not have the necessary "four wires" used for chip select signals in "encoded ***quad*** chip select mode," and therefore, it is impossible for the dual-rank RDIMMs to ever implement Encoded QuadCS mode. (*Id.* at 13.) As support, Micron cites to Dr. Stone's testimony that "[t]he module does not have the connectivity required by this chip to operate" in such a mode because those dual-rank modules "only have two wires" and you cannot use the RCD to operate "four wires when you only have two." (*Id.* (citing Trial Tr. at 794:3-4; 681:7-9).)

Micron further argues that not only are its dual-rank RDIMMs incapable of operating in an Encoded QuadCS mode, but that Netlist also presented no evidence that its dual-rank RDIMMs are reasonably capable based on the *TGIP* factors. (Dkt. No. 159 at 13-14 (citing *INVT SPE LLC v. Int'l Trade Comm'n*, 46 F.4th 1361, 1371–77 (Fed. Cir. 2022) ("[S]ome apparatus claims [] require an infringing device to actually perform and operate according to the functional terms recited in the claims" while "other apparatus claims [] require only capability. . . . Because we require claim limitations to have some teeth and meaning, proof of reasonable capability of performing claimed functions requires, at least as a general matter, proof that an accused product—when put into operation—in fact executes all of the claimed functions at least some of the time or at least once in the

[4] Micron argues that Mr. Cyr's testimony regarding the devices being wired per JEDEC specifications actually supports Micron's position that dual-rank modules cannot infringe because they do not have the necessary wires for Encoded QuadCS mode. (Dkt. No. 178 at 9.)

claim-required environment.").) Specifically, Micron argues that (1) there is no evidence that Micron intended or anticipated that consumers could or would modify the dual-rank RDIMMs to used encoded quad chip select mode, (2) no evidence shows that its dual-rank RDIMMs were "designed to be altered or assembled" to use encoded quad chip select mode before operation, (3) its technical data sheets [redacted] and (4) using Encoded QuadCS mode cannot serve any functional purpose beyond what was already accomplished by its configurations using Direct DualCS mode. (Dkt. No. 159 at 14-16.) Consequently, Micron argues that the Court should conclude that no substantial evidence exists to show that the accused dual-rank RDIMMs infringe claim 16. (*Id.* at 16.)

In response, Netlist argues that *TGIP* is "off point" because there, the court found no infringement since the accused product would require actual reprogramming in order to infringe the claims. (Dkt. No. 173 at 22 (citing *TGIP, Inc. v. AT&T Corp.*, 527 F. Supp. 2d 561, 573 (E.D. Tex. 2007) ("The basic question is whether AT&T's computerized system infringes a patent claim because it is possible that AT&T could reprogram the system in ways that would infringe the claim.").) Netlist argues that the court expressly distinguished its facts from those in *Intel Corp. v. United States International Trade Commission*, stating that "[t]his is not the same issue as in *Intel Corp*., where . . . the accused device was capable of operating in the same mode as the invention." (Dkt. No. 173 at 22 (citing *TGIP*, 527 F. Supp. 2d at 574) (citing 946 F.2d 821, 832 (Fed. Cir. 1991).) Netlist further contends that substantial evidence at trial supports a finding that all accused DDR4 DIMMs, including dual-ranked RDIMMs, can be placed into Encoded QuadCS mode if the host instructs them to do so and without the need for modification. (Dkt. No. 173 at 22.) Netlist contends this is particularly true given that when Micron's own counsel asked its

infringement expert, Dr. Stone, on direct examination whether "the Micron products" are "capable of using [direct quad or encoded quad mode]," Dr. Stone testified equivocally to the jury that "the chip may be able to go into the mode, but I doubt it." (Dkt. No. 185 at 8 (citing Trial Tr. at 793:19-794:4).)

Netlist contends that this is a classic battle-of-the-experts case where the jury, after being presented with both sides, found in favor of Netlist. (*Id.*) Netlist argues that the verdict should not be disturbed because the Court should respect the jury's fact-finding role in battle-of-the-expert scenarios. (*Id.* (citing e.g., *Anascape, Ltd. v. Nintendo of Am., Inc.*, No. 9:06-CV-158, 2008 U.S. Dist. LEXIS 127518, at *8 (E.D. Tex. 2008) ("This case presented the classic 'battle of the experts,' and the jury clearly chose to believe Anascape's infringement expert.")).

The Court finds that there is substantial evidence to support infringement under Netlist's Encoded QuadCS mode theory. In addition to the evidence discussed above, the jury heard Dr. Mangione-Smith testify that [redacted] (Trial Tr. at 346:14-347:1.) The jury also heard Dr. Stone admit that [redacted]. (*Id.* at 744:14-20.) Further, Dr. Mangione-Smith explained that the dual-rank RDIMMs are capable of using Encoded QuadCS mode because the "if the host tells it to go into encoded quad chip select, it will do it." (*Id.* at 347:2-14.) Micron's own expert, Dr. Stone, admitted so during his direct examination when Micron's counsel asked whether Micron's products are capable of using Encoded QuadCS mode. (*Id.* at 793:19-794:4). In that moment, Dr. Stone admitted that "the chip may be able to go into the mode, but I doubt it." (*Id.*) The jury was entitled to credit Netlist's evidence and apparently did. *See Gomez v. St. Jude Med. Daig Div. Inc.*, 442 F.3d 919, 933 (5th Cir. 2006) ("[The Court] must draw all reasonable inferences and resolve all conflicting evidence in favor of [the verdict].").

In conclusion, the Court finds that the jury could reasonably find infringement of claim 16's limitation requiring that output signals control more devices and ranks than input signals. Accordingly, Micron's request for judgment as a matter of law of non-infringement of the '912 Patent with respect to the accused dual-rank RDIMM products should be denied.

B. The '417 Patent

Micron contends it is entitled to judgment as a matter of law of non-infringement of all the Asserted Claims (Claims 1-2, 8, and 11-14) of the '417 Patent on the grounds that Netlist failed to show that the accused DDR4 LRDIMMs satisfy the "CAS latency limitation" in claim 1 based on the Court's constructions of "overall CAS latency" and "actual operational CAS latency." (Dkt. No. 159 at 24.)

In the '417 Patent, the "CAS latency limitation" in Claim 1 requires:

> wherein data transfers through the circuity are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

(JX-01 at 42:63-67, Claim 1 of the '417 Patent.)

In the Court's Claim Construction Order, the Court construed "overall CAS latency" of a memory module as "the delay between: (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module." (Dkt. No. 173-6 at 34.) The Court also construed "actual operational CAS latency" of a memory device as "the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device." (*Id.*)

Micron contends that Netlist failed to prove that the CAS latency limitation is satisfied because Dr. Mangione-Smith never identified any "starting point or ending point for his analysis of the CAS latency terms and the CAS latency limitation." (Dkt. No. 159 at 24-25.) Micron further

contends that Netlist cannot point to any evidence at trial regarding "the delay between (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module," nor can Netlist point to any evidence that purports to be "the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device." (*Id.* at 25.) Consequently, Micron contends that because Dr. Mangione-Smith failed to identify the delay period for "overall CAS latency" to compare to the delay period for "actual operational CAS latency," he failed to prove the CAS latency limitation for either a read command or a write command. (*Id.*) Ultimately, Micron's position is that Dr. Mangione-Smith provided an incorrect measure of "overall CAS latency" by analyzing the time between when a command is "executed by" the memory module and when data is "made available to or from" the *data buffer* contained *within* the memory module, not the *actual* memory module recited in the Court's Claim Construction Order. (Dkt. No. 159 at 22-23, 26.)

Netlist responds that substantial evidence supports the jury's infringement verdict. (Dkt. No. 173 at 23-24.)[5] First, Netlist begins by contending that the jury could reasonably have found that: (1) for the memory module, the "starting point" is when the RCD receives the command and the "end point" is when the read data is outputted from the data buffer and thus made available

[5] Netlist also claims that Micron's Motion improperly rehashes its *Daubert* motion, which the Court denied. (Dkt. No. 173 at 23-24 (citing *Rembrandt Wireless Techs., LP v. Samsung Elecs. Co.*, No. 2:13-CV-213-JRG, 2016 WL 362540, at *3 (E.D. Tex. Jan. 29, 2016) (noting that the Federal Circuit has held that a JMOL is not the appropriate context for renewing attacks on an expert's methodology), *aff'd,* 853 F.3d 1370 (Fed. Cir. 2017)).) Micron admits in its Motion that it filed a *Daubert* motion and a summary judgment motion identifying how Dr. Mangione-Smith "improperly focuses on data buffer timing," which is similar, if not the same, as the issue it raises now. (Dkt. No. 159 at 26.) Accordingly, to the extent that Micron attacks Dr. Mangione-Smith's methodology in this Motion, the Court rejects such attempts as improper. One such example is when Micron attacks Dr. Mangione-Smith's analysis, stating that the analysis "cannot be correct" because he used the "data buffer" circuit "within a memory module" rather than the "actual memory module." (Dkt. No. 159 at 26.) This is an improper attack on Dr. Mangione-Smith's methodology. Nonetheless, the Court will review the Motion to the extent that Micron challenges the sufficiency of the evidence.

from the memory module to the memory controller; and (2) for the DRAM device, the "starting point" is when the DRAM receives the read command, a time after the RCD receives the command; and the "end point" is when the read data is outputted by the DRAM and therefore made available from the DRAM to the data buffer. (Dkt. No. 173 at 25-26.) As support, Netlist cites Dr. Mangione-Smith's testimony explaining how the read and write data flows through the data buffer between the memory device and the host:

> Q. And so for a read command, what's the flow of data look like?
>
> A. So for a read command, the memory controller will send it first to the RCD, and that's when the module gets the command. And then subsequent -- after that, the RCD will send read commands to the individual DRAMs.
>
> Q. And what does the DRAM do when it gets a read command?
>
> A. Well, it responds to that command, pulls out the data that's being asked for, and provides it to the data buffer.
>
> Q. And what happens after that?
>
> A. Then the data buffer holds onto that data for a short period of time, that's the delay, and then it provides it to the host, to the memory controller.

(Dkt. No. 173 at 25 (citing Trial Tr. at 393:1-13). Netlist contends this is supported by Dr. Stone's testimony when Dr. Stone agreed that "the actual latency of the memory device is between when the command is received by the device and when the read data is at the output of the device in the read context" and that "the output of the DRAM device means the point at which the data is usable by the module." (Dkt. No. 173 at 25 (citing Trial Tr. at 760:17-25).)

Netlist then notes that Dr. Mangione-Smith explained that "the actual operational CAS latency of the DRAM devices themselves is added to the buffer delay of the data buffers to produce the overall CAS latency." (Trial Tr. at 393:23-25.) Dr. Mangione-Smith further testified that the

[redacted]

[redacted]

In addition, Netlist notes that Dr. Mangione-Smith points to testimony from Micron's witnesses to show that some amount of delay occurs when the data buffer holds on to the read data for a short period of time. (*Id.* at 26 (citing, e.g., Trial Tr. at 392:15-20 ("Q. And what did Mr. Ross say about whether the data buffers they put into the Micron products added some delay to those data transfers? A. Well, we saw some registers in that circuitry, and Mr. Ross was asked about the data buffers, and he agreed that they would add latency to data transfers."); 396:3-12; 536:23-537:1 ("Q. So on LRDIMMs, does the addition of data buffers add delay to data transfers between the memory controller and the DRAMs? A. [Mr. Ross:] Yes."); 561:17-22 (Mr. Cyr testifying that the "data buffer will introduce a propagation delay").) Based on this testimony, Netlist contends that a jury could have reasonably found that this delay in data buffer alone would establish that the overall CAS latency of the memory module is greater than the actual operational CAS latency of the DRAMs. (Dkt. No. 173 at 26.)

Netlist contends, moreover, that additional substantial evidence supports the jury's verdict. (*See* Dkt. No. 173 at 27-29.) For example, Netlist claims that Dr. Stone "admitted on cross-examination that the CAS latency limitation was met for read operations." (*Id.* at 28.) The relevant portion of that cross-examination went as follows:

> Q. … The actual latency is when the data, the read data is output from the DRAM such that it's usable by the device. Correct? Usable by the module.
>
> A. That's correct.
>
> Q. And the overall latency is that plus the buffer. Correct?
>
> A. That's correct.
>
> ***Q. And for read commands, the overall module delay will always be greater than the actual delay of the memory device. Correct?***
>
> ***A. That's correct.***

. . .

Q. It literally says that the overall latency is greater than the actual latency of the memory device. Correct?

A. There's a context in which it's correct, yes.

. . .

Q. The overall is always greater in the read context.

A. That's correct.

Q. That's for all of Micron's accused LRDIMMs. Correct?

A. That's correct.

(Trial Tr. at 763:14-24, 764:4-6) (emphasis added). From this exchange, Netlist contends that a reasonable jury would understand that "overall latency" and "actual latency" refer respectively to the "overall CAS latency" of the memory module and the "actual operational latency" of the memory device cited in the claims and consequently, the jury could arrive at the factual determination that Micron's products meet the CAS latency limitation for at least the "read" operation. (Dkt. No. 173 at 29.)

Micron responds, nonetheless, that Netlist cannot prove infringement of the CAS latency limitation because Netlist failed to provide any evidence at trial of the timing requirement of "overall CAS latency" and "actual operational CAS latency" as those terms are construed by the Court. (Dkt. No. 178 at 9.) Micron contends that Netlist's *post hoc* attempt to add that evidence now, by arguing the timing of the "starting point" and "end point" is improper since it was not offered at trial. (*Id.* at 9-10.) Netlist argues, however, that Micron is wrong that Netlist did not offer any contention at trial of the "starting point" and "end point" for the "overall CAS latency" and "actual operational CAS latency" because Netlist pointed to extensive evidence from Dr. Mangione-Smith and Dr. Stone. (Dkt. No. 185 at 8 (citing *e.g.*, Trial Tr. at 393:1-13 (discussing the flow of data through the data buffer and between the memory device and the host)).)

Micron further contends that Netlist's argument that a jury may have understood Dr. Stone's cross-examination testimony as referring to the Court's construction of the claim terms is also improper speculation and not substantial evidence because Dr. Stone was "actually and strategically asked about unclaimed latency terms that Netlist's counsel had defined differently." (*Id.* at 10.) Netlist responds not only by claiming that Micron does not explain how the terms used in cross-examination are inconsistent with the claimed terms, but also by demonstrating that "Dr. Stone used these terms interchangeably throughout his direct examination." (Dkt. No. 185 at 8 (citing e.g., Trial Tr. at 685:16-686:3 ("Q. Please explain to the jury the concept of ***CAS latency*** as it's used in this patent. A. Okay. I wanted to point to the word 'latency'. What's latency? That's a delay. It's a difference in time. So each latency starts at a particular time and ends at a particular time. And these are crucial for the operation of a memory module. Okay? So we have latency in our mind. There are two types of latency. We have an ***overall*** and we have an ***actual operational***.") (emphasis added).)

Having reviewed the Motion, the subsequent briefing, and the applicable trial exhibits, the Court finds that a reasonable jury could determine that Micron's products meet the CAS latency limitation. In this case, the CAS latency limitation in Claim 1 of the '417 Patent requires that the overall CAS latency of the memory module be greater than the actual operational CAS latency of the memory devices. (*See* JX-1 at 42:63-67.) During the trial, the jury heard testimony from several witnesses, including Dr. Mangione-Smith, Mr. Cyr, Mr. Ross, and Dr. Stone, that would allow them to find that the overall CAS latency of the memory module in Micron's products is greater than the actual operational CAS latency in the memory devices.

As a preliminary matter, the jury heard Dr. Mangione-Smith explain how the CAS latency limitation is met. (*See e.g.*, Trial Tr. at 390:14-399:10; 402:5-405:15; 416:16-420:10.).) Specifically, the jury heard Dr. Mangione-Smith begin testifying about this limitation by

explaining the Court's construction of "actual operational CAS latency" and "overall CAS latency" and the requirement that the "overall CAS latency" be greater than the "actual operational CAS latency" of the individual DRAM chips. (Trial Tr. at 390:14-391:23.) Dr. Mangione-Smith subsequently discussed testimony from Mr. Ross where Mr. Ross stated that the data buffers put into Micron's products added latency to the data transfer. (Trial Tr. at 392:15-20; 536:23-537:1 ("Q. So on LRDIMMs, does the addition of data buffers add delay to data transfers between the memory controller and the DRAMs? A. [Mr. Ross:] Yes.").) Dr. Mangione-Smith also discussed testimony from Micron's engineers, such as Mr. Cyr, that stated the data buffers actually add the flow of data for read and write commands. (Trial Tr. at 396:3-12; 561:17-22 ("Q. And will add a time delay in its flow from the – for example, from the host system to the DRAM? A. The -- the data buffer will introduce a propagation delay. Q. And that's a time delay? A. Time delay. Correct.").) The jury further heard Dr. Mangione-Smith testify that the "actual operational CAS latency of the DRAM devices themselves is added to the buffer delay of the data buffers to produce the overall CAS latency." (Trial Tr. at 393:23-25.) Dr. Mangione-Smith supported this testimony using source code. (*See e.g.*, *id.* at 416:16-25.) From this testimony, the Court agrees with Netlist that a jury could reasonably conclude that this delay in the data buffer establishes that the overall CAS latency of the memory module is greater than the actual operational CAS latency of the DRAMs. (*See, e.g.*, Trial Tr. at 393:23-25; 416:16-25; Dkt. No. 173 at 26.) Given that Dr. Stone admitted he did not analyze the applicable source code (*see* Trial Tr. at 708:8-11), a reasonable jury could also have given less weight to Dr. Stone's testimony on this point, to the extent that he reached a different conclusion than Dr. Mangione-Smith.

In addition to the testimony from Dr. Mangione-Smith, Mr. Ross, and Mr. Cyr, the jury heard Micron's own expert witness, Dr. Stone, admit that the CAS latency limitation was met.

Specifically, the jury heard Dr. Stone admit that "for read commands, the overall module delay will always be greater than the actual delay of the memory device" and also that for "all of Micron's accused LRDIMMs," the "overall is always greater in the read context." (*Id.* at 763:14-24, 764:14-18.) While Micron claims that Netlist strategically asked Dr. Stone about unclaimed latency terms instead of the claimed "actual operational CAS latency" and "overall CAS latency" terms, the Court is not persuaded by Micron's argument. Dr. Stone used the terms "actual latency" and "overall latency" interchangeably with the claimed "actual CAS latency" and "overall CAS latency." As just another example, when Dr. Stone offered his contrary position, he stated that "[y]ou can actually measure that, 1.5 cycles longer for the ***actual*** than the ***overall***" (Trial Tr. at 691:9-10.) Consequently, the admission by Dr. Stone that the overall module delay will always be greater than the actual delay of the memory device for "read" commands is sufficient evidence to support the jury's verdict.

Ultimately, the Court finds that substantial evidence supports the jury's finding that the CAS latency limitation, which requires that the overall CAS latency of the memory module be greater than the actual operational CAS latency of the memory devices, is met. Accordingly, the Court finds that judgment as a matter of law for non-infringement of the '417 Patent is not appropriate under the arguments Micron's proffers in its Motion.

IV. CONCLUSION

For the reasons stated herein, the Court finds that Micron's Motion (Dkt. No. 159) should be and hereby is **DENIED**.

The parties are directed to jointly prepare a redacted version of this Order for public viewing and to file the same on the Court's docket as an attachment to a Notice of Redaction within five (5) business days of this Order.

So ORDERED and SIGNED this 11th day of June, 2025.

RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE